

# Ultra-small 2.5A Load Switch with Discharge

## Description

The AM6U1125 is a 17mΩ, 2.5A single-channel load switch that switches 1.0V to 5.5V power rails. It contains two overcurrent protection modes and configurable slew rate control.

The product is packaged in an ultra-small 1.0x1.6mm package.

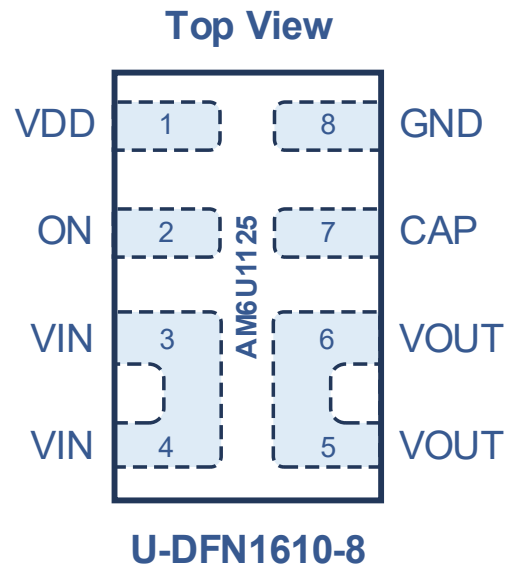
## Features

- 1.0x1.6x0.55mm U-DFN1610-8 package
- 17mΩ RDS<sub>ON</sub> while supporting 2.5A
- Discharges load when off
- Two Over Current Protection Modes
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- RoHS Compliant / Halogen-Free / Pb-Free
- Operating Temperature: -40°C to 85°C
- Operating Voltage: 2.5V to 5.5V

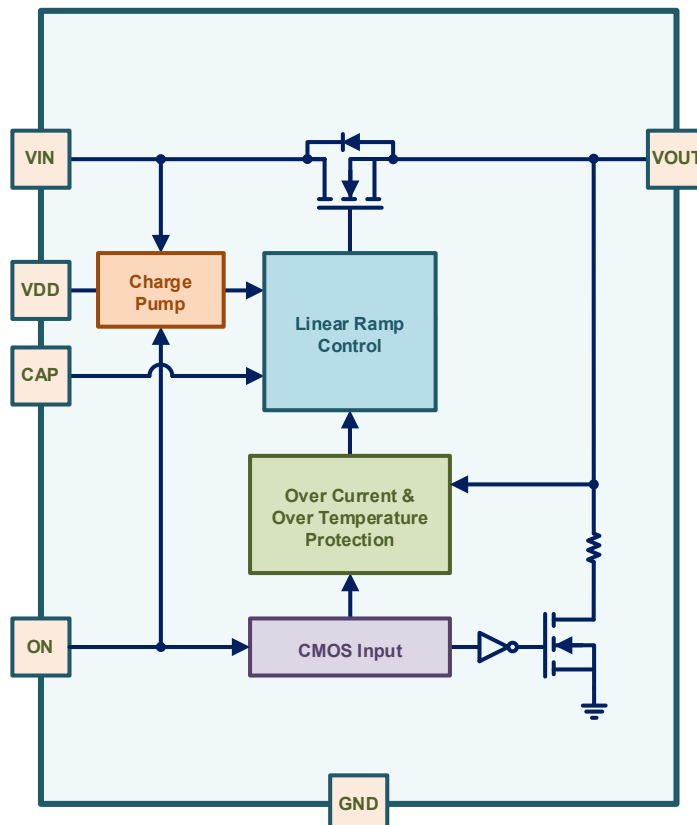
## Applications

- Smartphones
- Tablets
- Notebooks

## PIN Configuration



## Functional Block Diagram

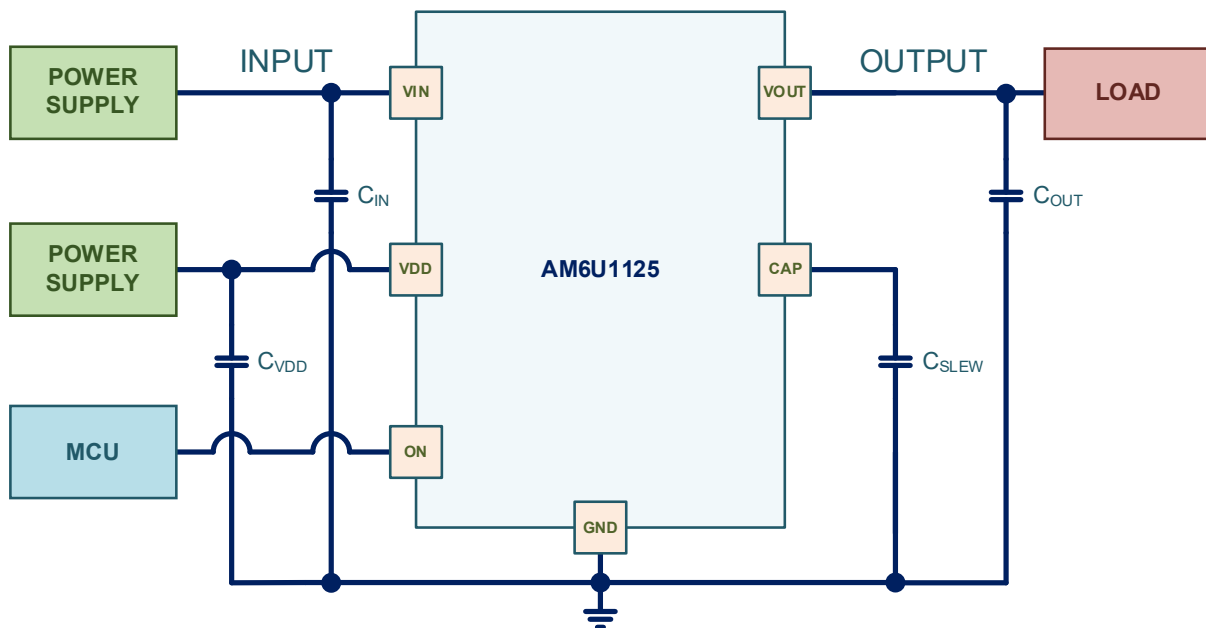




### Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	Power supply. Assumes a 0.1 $\mu$ F or larger decoupling capacitor.
2	ON	Input	Turns on load switch, active HI. There is an internal pull-down circuit to GND (~5 M $\Omega$ ).
3, 4	VIN	MOSFET	Drain terminal connection for the load switch. Connect at minimum a low-ESR 10 $\mu$ F capacitor from this pin to GND.
5, 6	VOUT	MOSFET	Source terminal connection of the load switch. Connect a low-ESR capacitor from this pin to GND.
7	CAP	Input	Connects to a low-ESR ceramic capacitor to set the V <sub>OUT</sub> slew rate.
8	GND	GND	Ground.

### Typical Application Circuit





**Absolute Maximum Ratings**

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Power Supply		—	—	7	V
T <sub>S</sub>	Storage Temperature		-65	—	150	°C
ESD <sub>HBM</sub>	ESD Protection	Human Body Model	2000	—	—	V
MSL	Moisture Sensitivity Level		1			
W <sub>DIS</sub>	Package Power Dissipation		—	—	0.4	W
MOSFET IDS <sub>PK</sub>	Peak Current from Drain to Source	For no more than 1ms with 1% duty cycle	—	—	3.5	A

**Electrical Characteristics**

T<sub>A</sub> = -40°C to 85°C unless otherwise stated. Typical values at T<sub>A</sub> = 25°C (unless otherwise stated).

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Power Supply	-40°C to 85°C	2.5	—	5.5	V
V <sub>IN</sub>	Switch Input Voltage		1.0	—	V <sub>DD</sub>	V
V <sub>IH</sub>	High Input Voltage on the ON pin		0.85	—	V <sub>DD</sub>	V
V <sub>IL</sub>	Low Input Voltage on the ON pin		-0.3	0	0.3	V
I <sub>SHDN</sub>	Input Shutdown Current	Disabled, I <sub>OUT</sub> = 0A	—	—	0.1	µA
I <sub>Q</sub>	Input Quiescent Current	Enabled, I <sub>OUT</sub> = 0A	—	25	50	µA
I <sub>OUT</sub>	Output Current	Continuous	0	—	2.5	A
I <sub>LIMIT</sub>	Active Current Limit <sup>1</sup>	MOSFET will automatically limit current when V <sub>OUT</sub> > 300 mV	—	4.2	—	A
	Short Circuit Current Limit <sup>1</sup>	MOSFET will automatically limit current when V <sub>OUT</sub> < 300 mV	—	1.1	—	
R <sub>DS(ON)</sub>	Switch ON Resistance	T <sub>A</sub> = 25°C; I <sub>OUT</sub> = 100mA	—	16.8	19	mΩ
		T <sub>A</sub> = 85°C; I <sub>OUT</sub> = 100mA	—	19.2	23	
R <sub>DIS</sub>	Discharge Resistance		180	215	250	Ω
R <sub>PULL-Down</sub>	ON Pull-Down Resistance		—	4.8	—	MΩ
t <sub>ON_Delay</sub>	ON Delay Time	50% ON to V <sub>OUT</sub> Ramp Start	—	250	500	µs
V <sub>OUT(SR)</sub>	Output Slew Rate	10% V <sub>OUT</sub> to 90% V <sub>OUT</sub>	Configurable <sup>2</sup>			V/ms
		Example: V <sub>DD</sub> = V <sub>IN</sub> = 5V, C <sub>SLEW</sub> = 3.9nF, C <sub>OUT</sub> = 10µF, R <sub>LOAD</sub> = 20Ω	—	3.35	—	
t <sub>ON</sub>	Total Turn On Time	50% ON to 90% V <sub>OUT</sub>	Configurable <sup>2</sup>			ms
		Example: V <sub>DD</sub> = V <sub>IN</sub> = 5V, C <sub>SLEW</sub> = 3.9nF, C <sub>OUT</sub> = 10µF, R <sub>LOAD</sub> = 20Ω	—	1.55	—	
t <sub>OFF_Delay</sub>	Off Delay Time	50% ON to V <sub>OUT</sub> Fall Start, V <sub>DD</sub> = V <sub>IN</sub> = 5.0V, R <sub>LOAD</sub> = 20Ω, no C <sub>OUT</sub>	—	6.5	—	µs
t <sub>FALL</sub>	V <sub>OUT</sub> Fall Time	90% V <sub>OUT</sub> to 10% V <sub>OUT</sub> , V <sub>DD</sub> = V <sub>IN</sub> = 5V, R <sub>LOAD</sub> = 20Ω, no C <sub>OUT</sub>	—	4.5	—	µs
C <sub>OUT</sub>	Output Load Capacitance	C <sub>OUT</sub> connected from V <sub>OUT</sub> to GND	—	—	500	µF
OTP	Overtemperature Protection <sup>1</sup>	Threshold	—	125	—	°C
		Hysteresis	—	25	—	

Notes:

- Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.
- Refer to typical timing parameter vs. C<sub>SLEW</sub> performance charts for additional information.



Typical Performance Characteristics

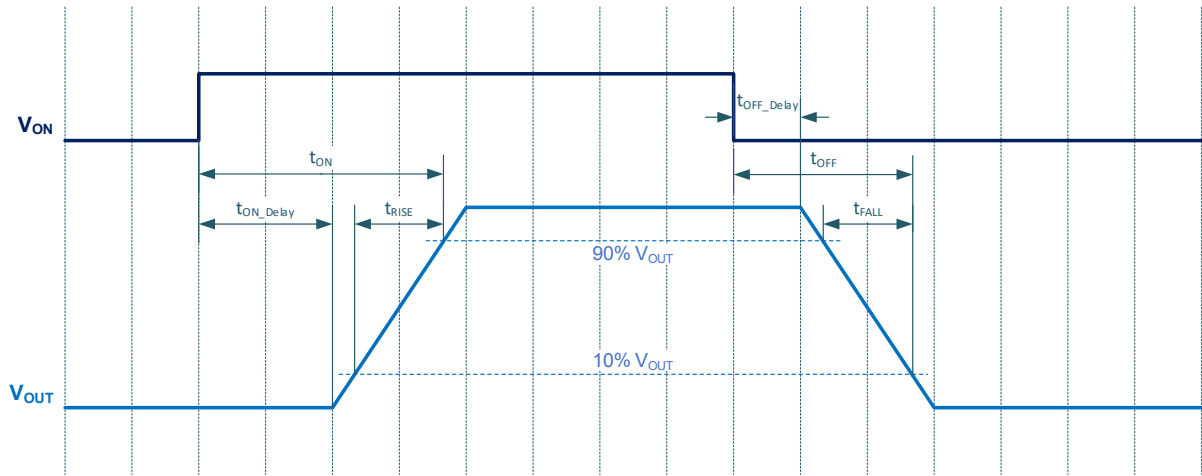


Figure 1. Basic Timing Parameters

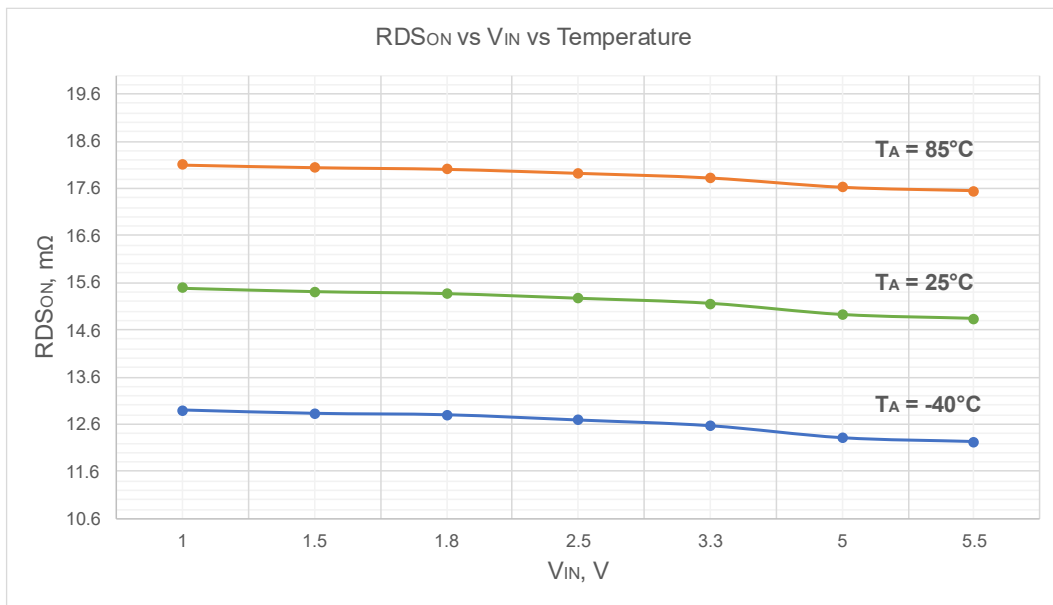


Figure 2.  $R_{DS(on)}$  vs.  $V_{IN}$  and Temperature at  $V_{DD} = 5.5\text{V}$  and  $I_{OUT} = 100\text{mA}$ .



# Ultra-small 2.5A Load Switch with Discharge

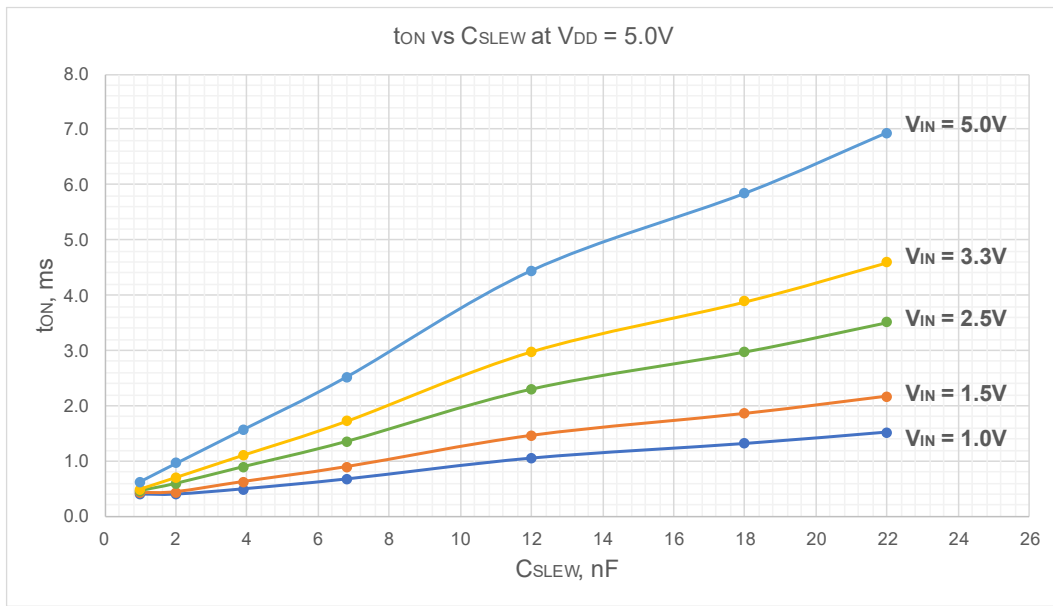


Figure 3. Total Turn On Time vs. CSLEW and VIN at VDD = 5.0V.

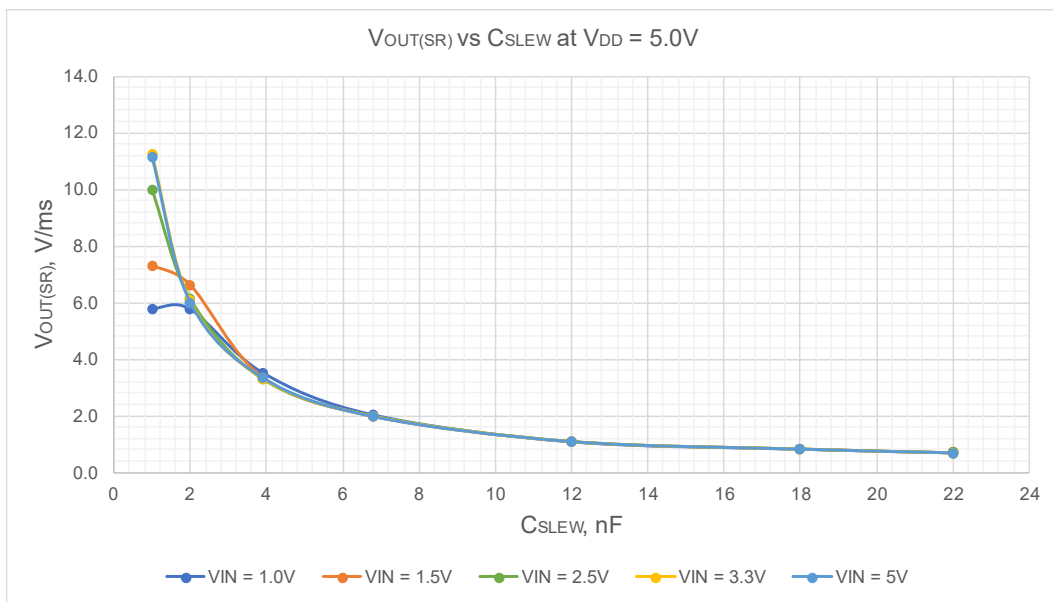


Figure 4. VOUT Slew Rate vs. CSLEW and VIN = 5.0V.



Application Information

Typical Operation

For correct operability per the AM6U1125 EC table a proper power-up sequence must be applied. Apply  $V_{DD}$  first, followed by  $V_{IN}$ , then ON signal to power-up the device. In order to control the inrush current from capacitive loads, set a desired linear output slew rate by placing a corresponding  $C_{SLEW}$  capacitor between CAP pin and GND. The greater the capacitor value at CAP pin, the slower the output ramp.

During operation, should a system fault occur,  $V_{IN}$  should be returned to Recommended Operating Conditions before the load switch is transitioned between its On and Off states to reduce out-of-spec transitional stress on the device.

Some typical operation waveforms are illustrated below.

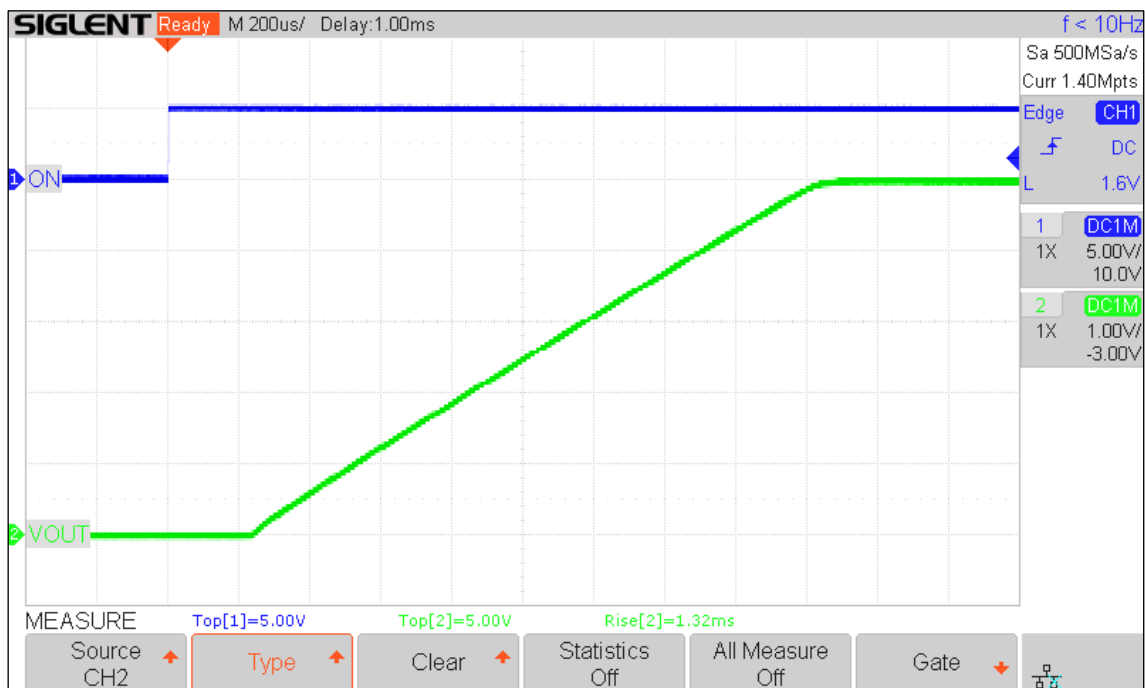


Figure 4. AM6U1125 Typical Power-Up Operation Waveform.  $V_{DD} = V_{IN} = 5V$ ,  $R_{LOAD} = 20\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{SLEW} = 3.9nF$

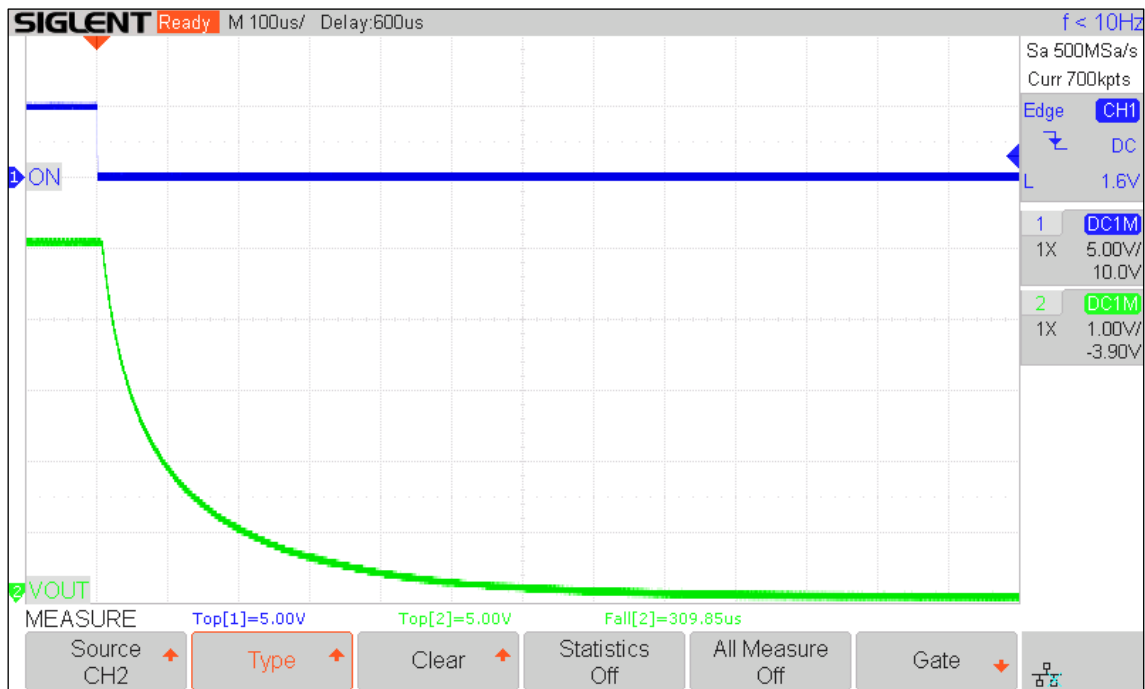


Figure 5. AM6U1125 Typical Power-Down Operation Waveform.  $V_{DD} = V_{IN} = 5V$ ,  $R_{LOAD} = 20\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{SLEW} = 3.9nF$

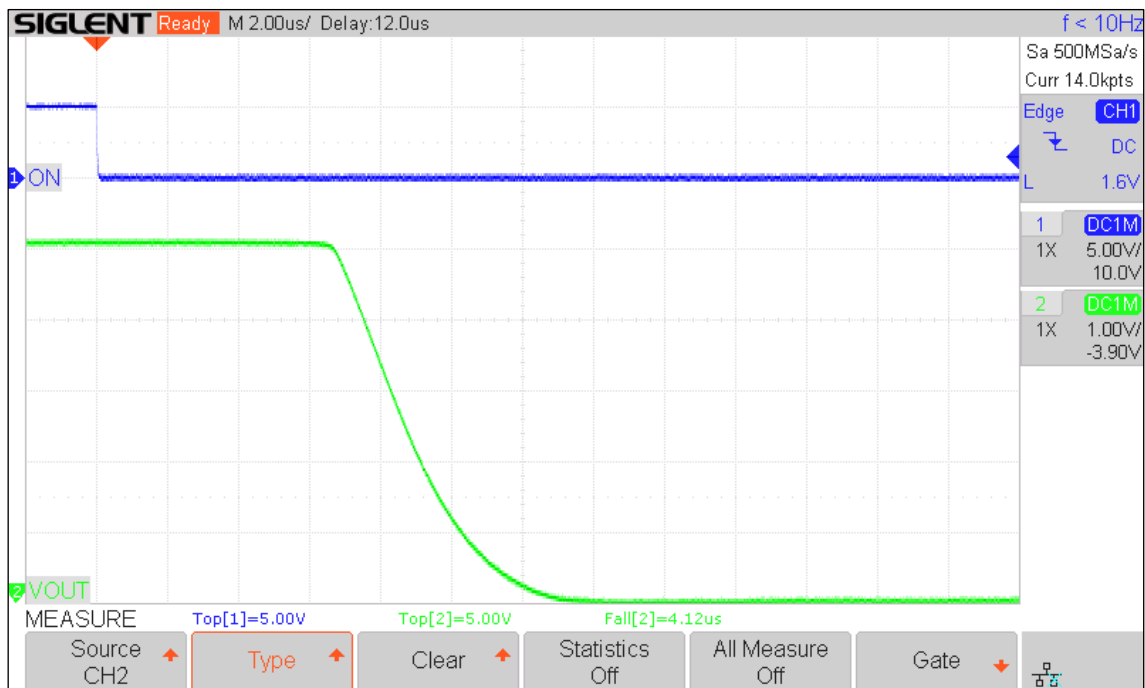


Figure 6. AM6U1125 Typical Power-Down Operation Waveform.  $V_{DD} = V_{IN} = 5V$ ,  $R_{LOAD} = 20\Omega$ , no  $C_{OUT}$ ,  $C_{SLEW} = 3.9nF$



### Overtemperature Protection

The AM6U1125 contains an overtemperature protection feature. If the internal junction temperature of the AM6U1125 reaches 125°C, such as during an overcurrent event, the FET is shut off completely so the die can cool. Once the die temperature reaches approximately 100°C Overtemperature Protection will disable and the FET will again be capable of conducting. This event will repeat for as long as the condition exists which causes the die to overheat.

### Current Limiting Operation

The AM6U1125 has two types of current limiting triggered by the VOUT pin voltage.

#### 1. Active Current Limit Mode

When voltage  $V_{OUT} > 300mV$  the output current is initially limited to the Active Current Limit ( $I_{ACL}$ ) specification listed in the Electrical Characteristics table. The ACL monitor's response time is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the load switch's  $I_{ACL}$  threshold.

If a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Overtemperature Protection circuit can be activated. If the die temperature exceeds the listed OTP Threshold specification, the FET is shut Off completely to allow the die to cool. When the die cools by the listed OTP Hysteresis temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

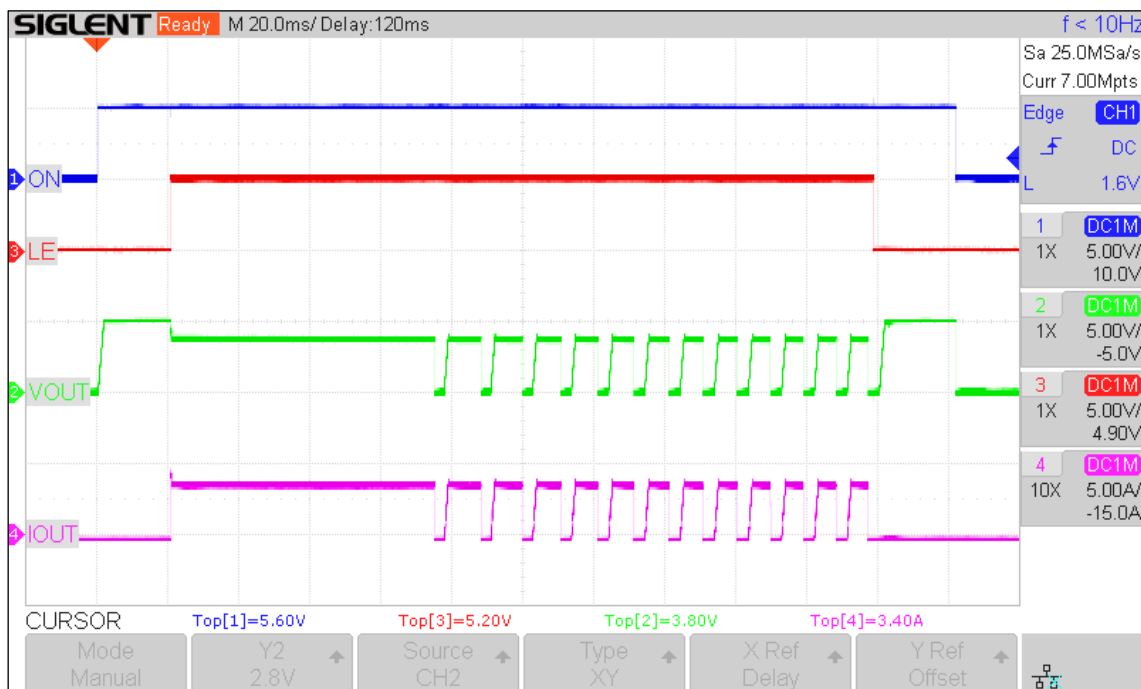


Figure 7. AM6U1125 ACL+OTP Operation Waveform.  $V_{DD} = V_{IN} = 5V$ ,  $R_{LOAD} = 20\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{SLEW} = 3.9nF$ . Load Enable signal applies an additional 1Ω of load.

An example of the AM6U1125 Active Current Limit is shown above. At initial turn-on of the IC the active current limit is sustained for longer before reaching the overtemperature limit. As the package is heated in subsequent ACL events the time held at the ACL level before triggering the overtemperature protection continues to decrease until it reaches a steady-state.



### 2. Short Circuit Current Limit Mode

The AM6U1125 also contains a short circuit current limit, which will trigger in the event that  $V_{OUT}$  is externally limited to 300mV or less due to an improper solder connection or similar defect on the same node as the  $V_{OUT}$  pin. During this event, the AM6U1125 will maintain the resistivity of the FET so as to limit the output current of the device to a typical value of 1A.

If the Short-circuit event is resolved the AM6U1125 will continue its voltage ramp per the slew rate set by the capacitor on the CAP pin.

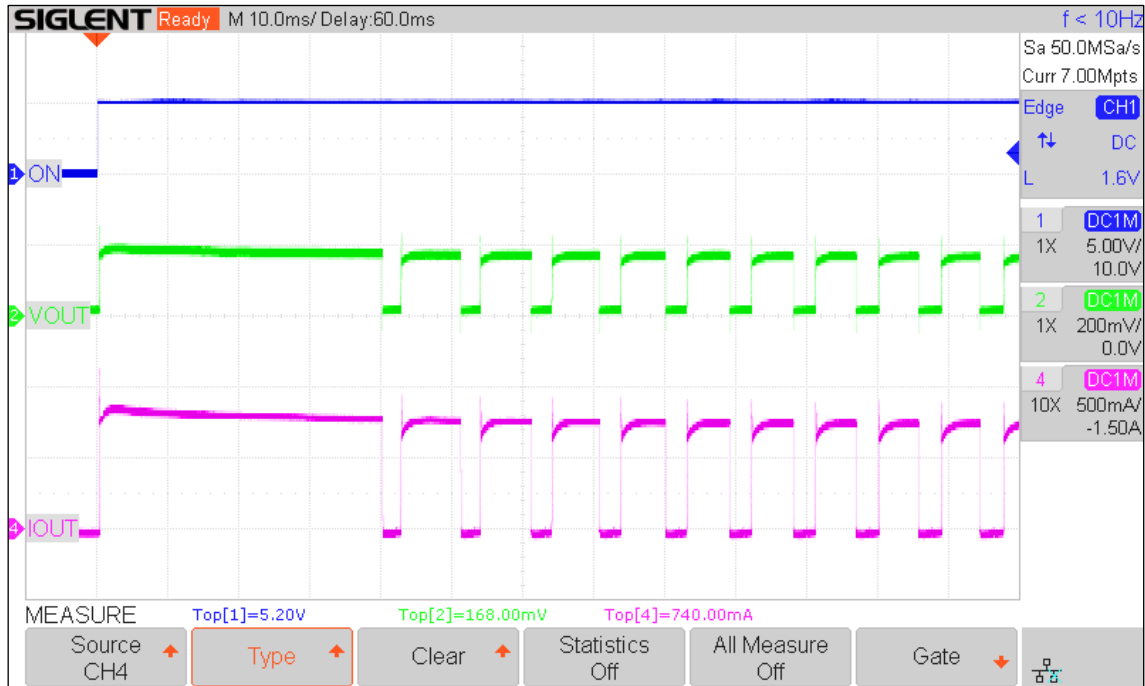


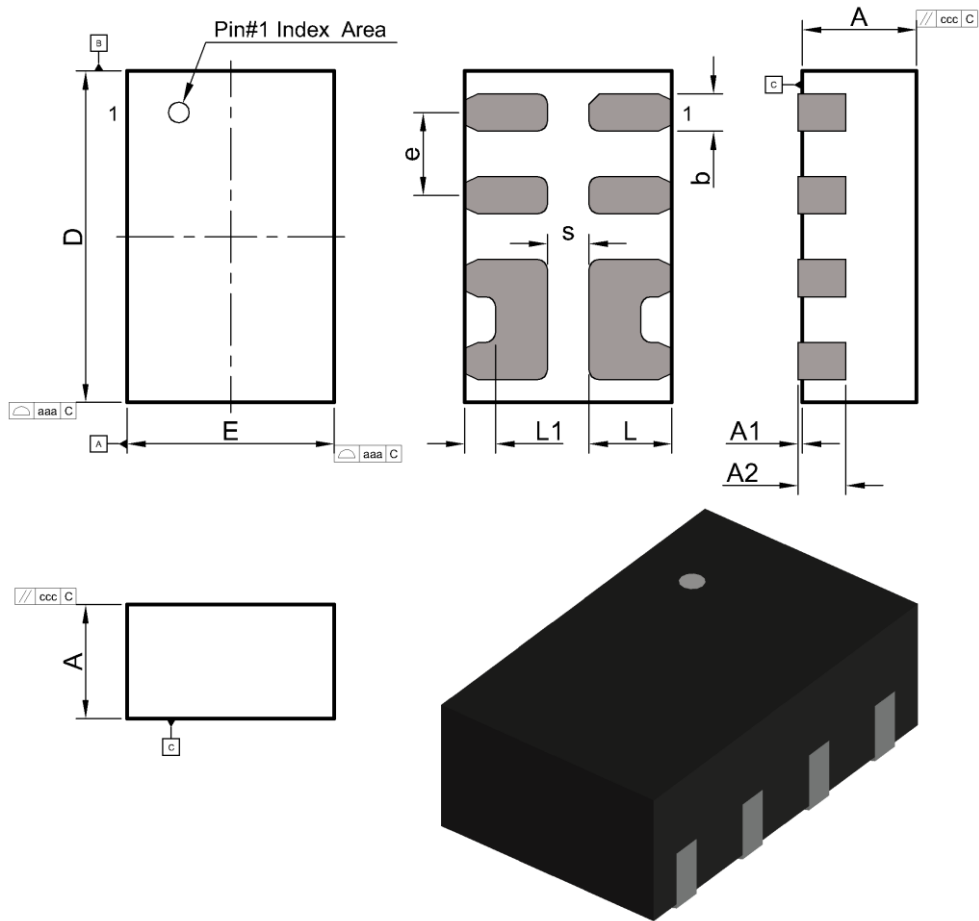
Figure 8. AM6U1125 SCL+OTP Operation Waveform.  $V_{DD} = V_{IN} = 5V$ ,  $R_{LOAD} = 0.2\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{SLEW} = 3.9nF$ .

Note: Depending upon factors such as  $V_{IN}$ , the shorted value of  $V_{OUT}$ , and ambient temperature, the AM6U1125 may or may not dissipate enough power to trigger the Overtemperature Protection within the circuit. If the overtemperature protection occurs the part will shut down and retry per the Overtemperature Detection description above.



Package Outline Dimensions

U-DFN1610-8



Symbol	Min.	Typ.	Max.	Symbol	Min.	Typ.	Max.
A	0.500	0.550	0.600	e	—	0.400	—
A1	0.010	—	0.000	L	0.375	0.400	0.425
A2	0.225	0.250	0.275	L1	0.125	0.150	0.175
b	0.155	0.180	0.205	s	—	0.200	—
D	1.550	1.600	1.650	aaa	—	0.050	—
E	0.950	1.000	1.050	ccc	—	0.050	—

All Dimensions in mm



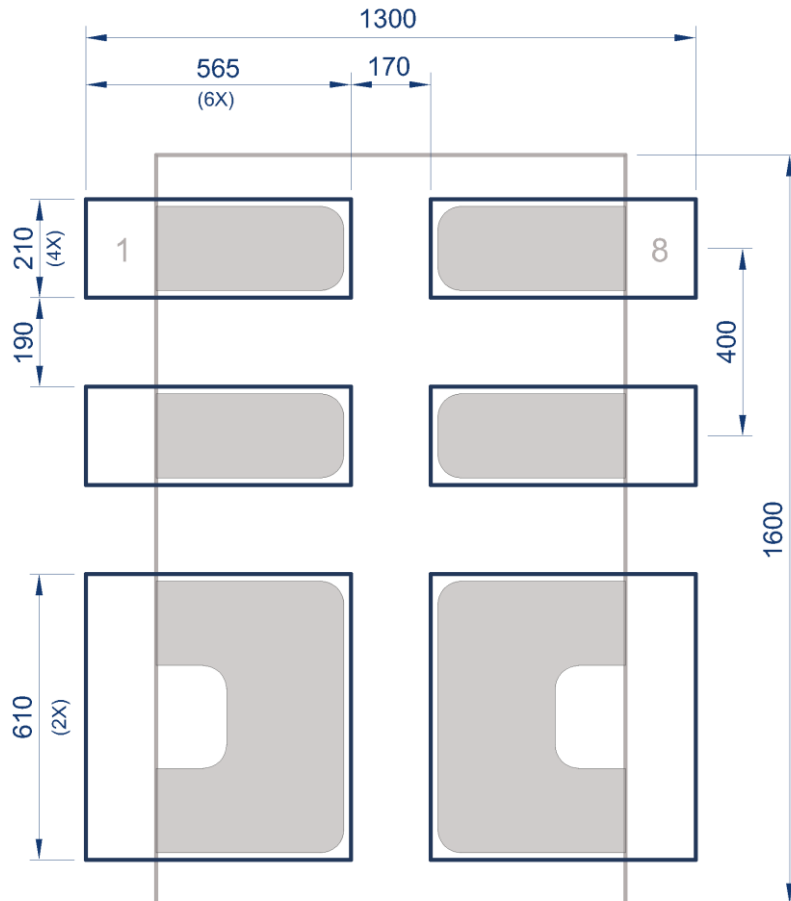
Package Top Marking



NN – Identification Code: A2  
Y – Year: 0~9  
W – Week: A~Z – 1~26 week  
a~z – 27~52 week, z represents 52 and 53 week  
N – Internal Code

Suggested Pad Layout

U-DFN1610-8



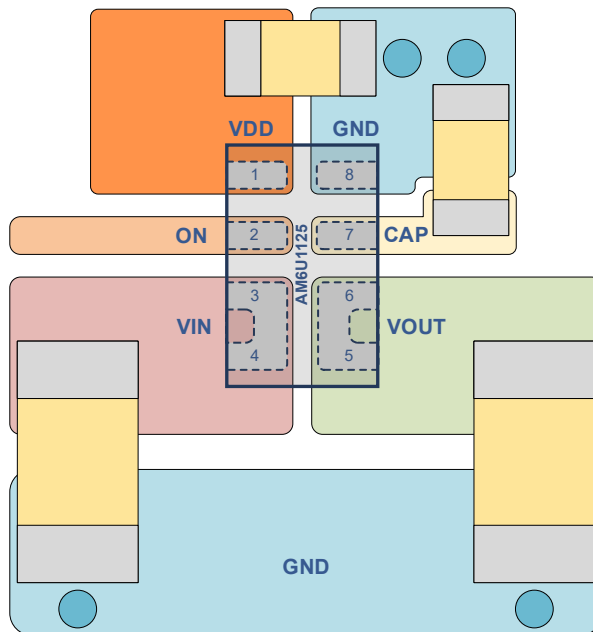


### Recommended Layout

It is important to have a proper PCB layout for high-performance device operation. The list below provides some basic rules for PCB layout.

- Connect a 0.1 $\mu$ F capacitor from VDD pin to GND. It should be placed as close to the device as possible.
- Place high-quality low-ESR input  $C_{IN}$  (10 $\mu$ F min) and output  $C_{OUT}$  capacitors close to the device VIN and VOUT pins to minimize the effects of parasitic inductance.
- Make sure to have a solid Ground connection.
- All traces should be as short, wide, and direct as possible.
- VIN and VOUT pins have the most heat dissipation during max current operations. Use polygon planes and/or 2 oz. copper for VIN and VOUT connections.

Example below illustrate described layout guidelines implementation.

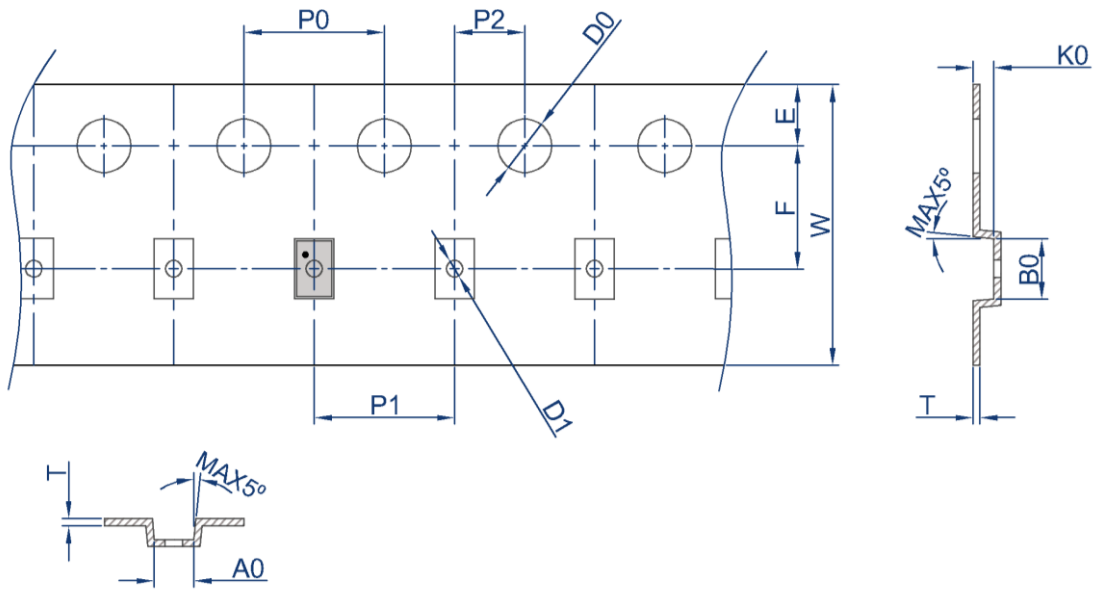




**Tape and Reel Specifications**

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
U-DFN1610-8	8	1.0 x 1.6 x 0.55	3000	3000	178/60	100	400	100	400	8	4

Package Type	A0	B0	K0	P0	P1	P2	T	D0	D1	E	F	W
U-DFN1610-8	1.12	1.72	0.7	4	4	2	0.2	1.55	0.5	1.75	3.5	8





**Revision History**

Date	Version	Change
November 9, 2023	Rev.001	Initial release
February 5, 2024	Rev.002	Updated pinout, EC table, graphs, and POD
June 6, 2025	Rev.003	Added Laser Marking section. Updated Recommended Layout



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