AM6U1404

4A Load Switch with Configurable Slew Rate Control

Description

The AM6U1404 is a 7mΩ, 4A single-channel load switch that switches 0.9V to 4.5V power rails. It contains two overcurrent protection modes and configurable slew rate control.
The product is packaged in a small 2.0x1.5mm package.

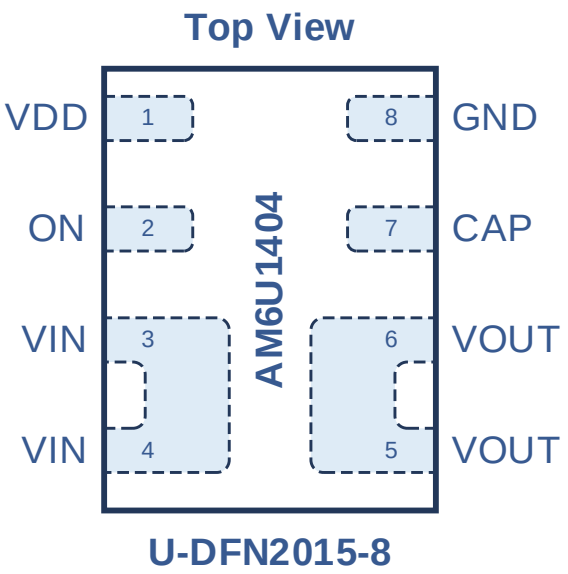
Features

- 2.0x1.5x0.55mm U-DFN2015-8 package
- Nominally supports up to 4A
- Two Over Current Protection Modes
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- RoHS Compliant / Halogen-Free / Pb-Free
- Operating Temperature: -40°C to 85°C
- Operating Voltage: 2.5V to 5.5V

Applications

- Smartphones
- Tablets
- Notebooks

PIN Configuration



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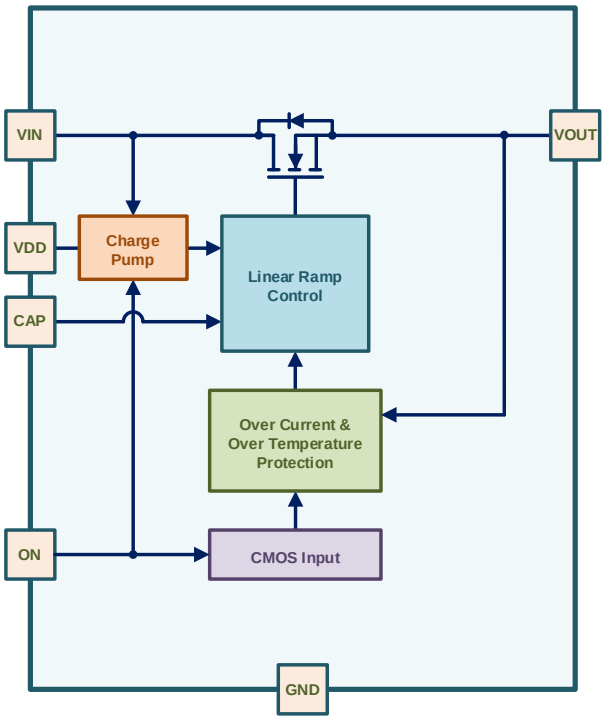
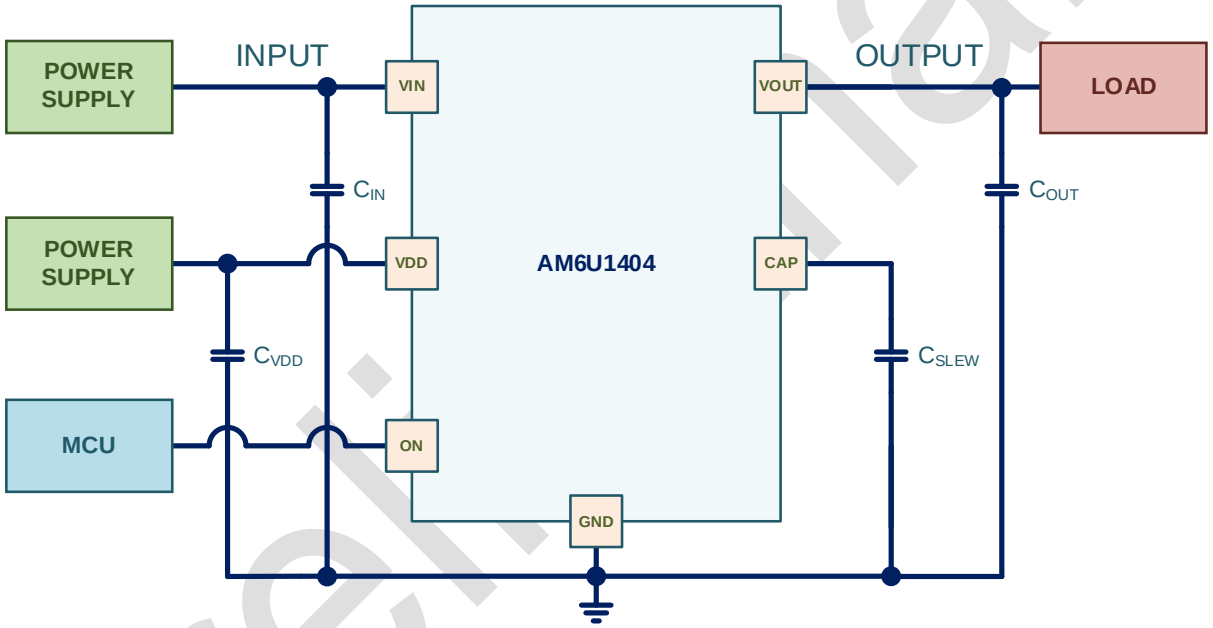
Functional Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	Power supply. Assumes a 0.1µF or larger decoupling capacitor.
2	ON	Input	Turns on load switch, active HI. There is an internal pull-down circuit to GND (~5 MΩ).
3 – 4	VIN	MOSFET	Drain terminal connection for the load switch. Connect at minimum a low-ESR 10µF capacitor from this pin to GND.
5 – 6	VOUT	MOSFET	Source terminal connection of the load switch. Connect a low-ESR capacitor from this pin to GND.
7	CAP	Input	Connects to a low-ESR ceramic capacitor to set the V_{OUT} slew rate.
8	GND	GND	Ground.

Typical Application Circuit



Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		—	—	7	V
T_S	Storage Temperature		-65	—	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	—	—	V
MSL	Moisture Sensitivity Level		1			
W_{DIS}	Package Power Dissipation		—	—	1	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	—	—	6	A

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise stated. Typical values at T_A = 25°C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply	-40°C to 85°C	2.5	—	5.5	V
V_{IN}	Switch Input Voltage	$V_{IN} \le V_{DD}$	0.9	—	4.5	V
V_{IH}	High Input Voltage on the ON pin		0.85	—	V_{DD}	V
V_{IL}	Low Input Voltage on the ON pin		-0.3	0	0.4	V
I_{SHDN}	Input Shutdown Current	Disabled, I_{OUT} = 0A	—	—	100	nA
I_Q	Input Quiescent Current	Enabled, I_{OUT} = 0A	—	25	50	µA
I_{OUT}	Current from Drain to Source	Continuous	—	—	4	A
I_{LIMIT}	Active Current Limit [1]	MOSFET will automatically limit current when V_{OUT} > 300mV	—	6.3	—	A
	Short Circuit Current Limit [1]	MOSFET will automatically limit current when V_{OUT} < 300mV	—	0.5	—	
RDS_{ON}	Switch On Resistance	T_A = 25°C; I_{OUT} = 100mA	—	7.5	8.5	mΩ
		T_A = 85°C; I_{OUT} = 100mA	—	8.3	10.0	
R_{Pull_Down}	ON pull-down resistance	V_{DD} = V_{ON} = 3.3V	—	5	—	MΩ
t_{ON_Delay}	On Delay Time	50% ON to V_{OUT} Ramp Start	—	230	500	µs
$V_{OUT(SR)}$	Slew Rate	10% V_{OUT} to 90% V_{OUT}	Configurable [2]			V/ms
		Example: V_{DD} = 5.5V, V_{IN} = 3.3V, C_{SLEW}= 3.9nF, C_{OUT} = 10µF, R_{LOAD} = 20Ω	—	4.7	—	
t_{ON}	Total Turn On Time	50% ON to 90% V_{OUT}	Configurable [2]			ms
		Example: V_{DD} = 5.5V, V_{IN} = 3.3V, C_{SLEW}= 3.9nF, C_{OUT} = 10µF, R_{LOAD} = 20Ω	—	0.82	—	
t_{OFF_Delay}	Off Delay Time	50% ON to V_{OUT} Fall Start, V_{DD} = 5.5V, V_{IN} = 3.3V; R_{LOAD} = 20Ω, no C_{OUT}	—	6	—	µs
C_{OUT}	Output Load Capacitance	C_{OUT} connected from VOUT to GND	—	10	500	µF
OTP	Overtemperature Protection [1]	Threshold	—	125	—	°C
		Hysteresis	—	25	—	°C

Notes:

1. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information.

Typical Performance Characteristics

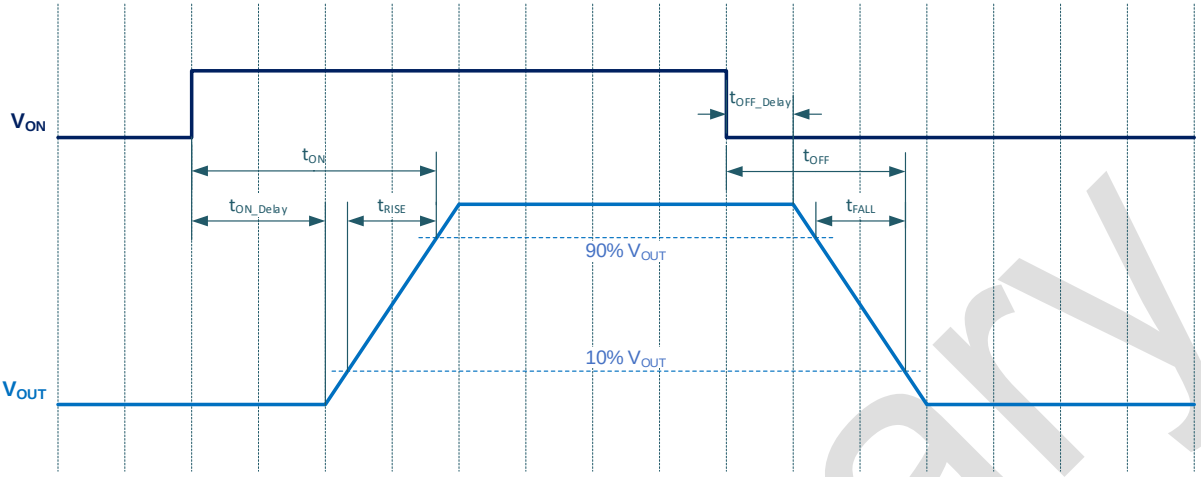


Figure 1. Basic Timing Parameters.

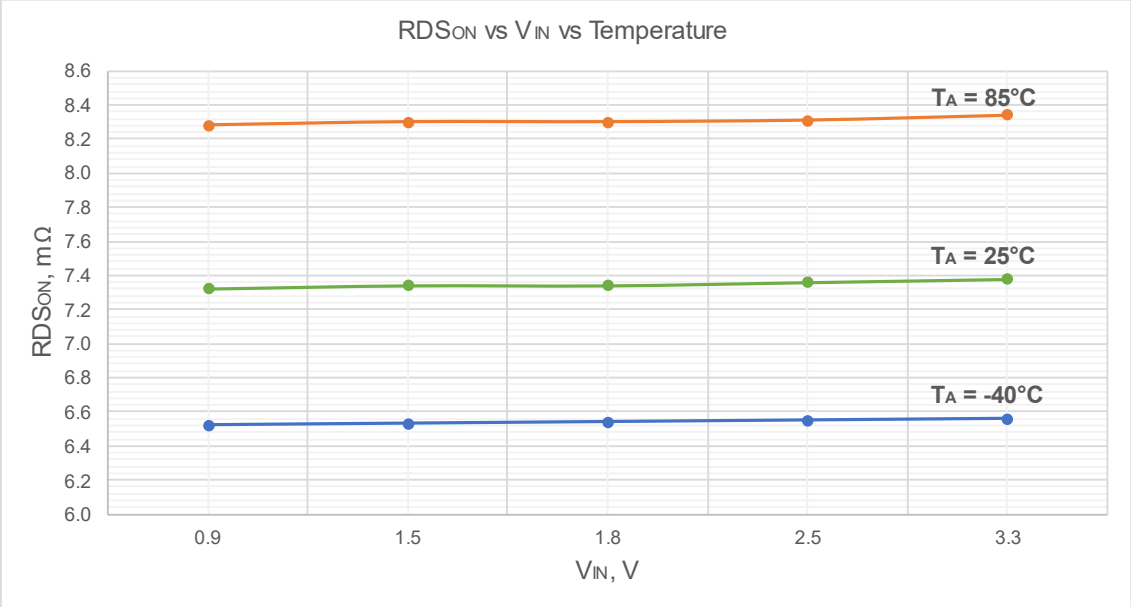


Figure 2. RDS_{ON} vs. V_{IN} and Temperature at V_{DD} = 3.3V and I_{OUT} = 100mA.

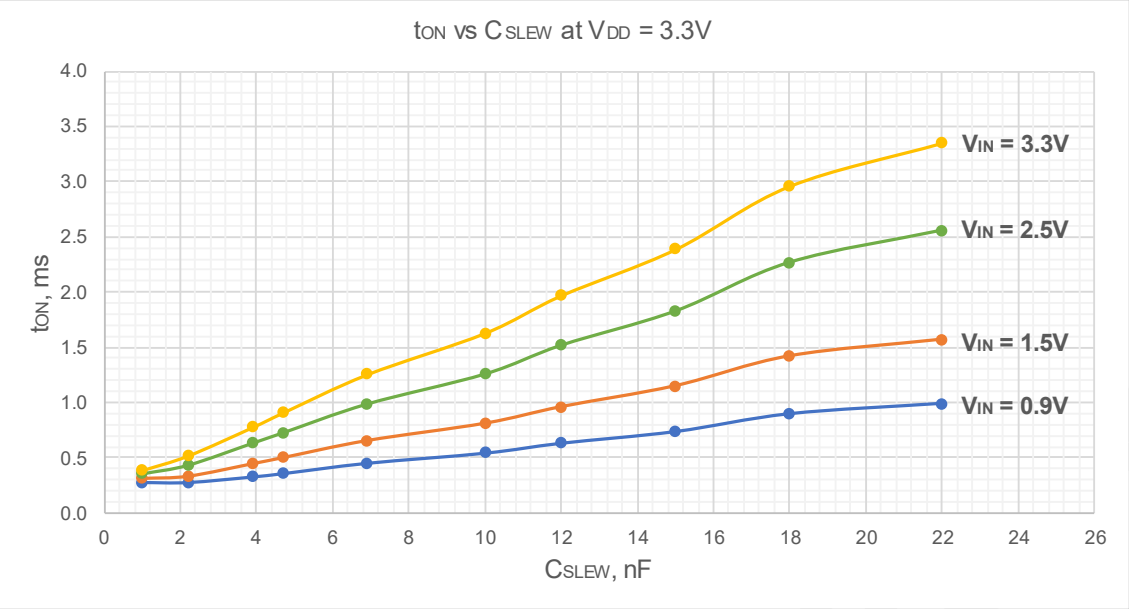


Figure 3. Total Turn On Time vs. C_{SLEW} and V_{IN} at V_{DD} = 3.3V.

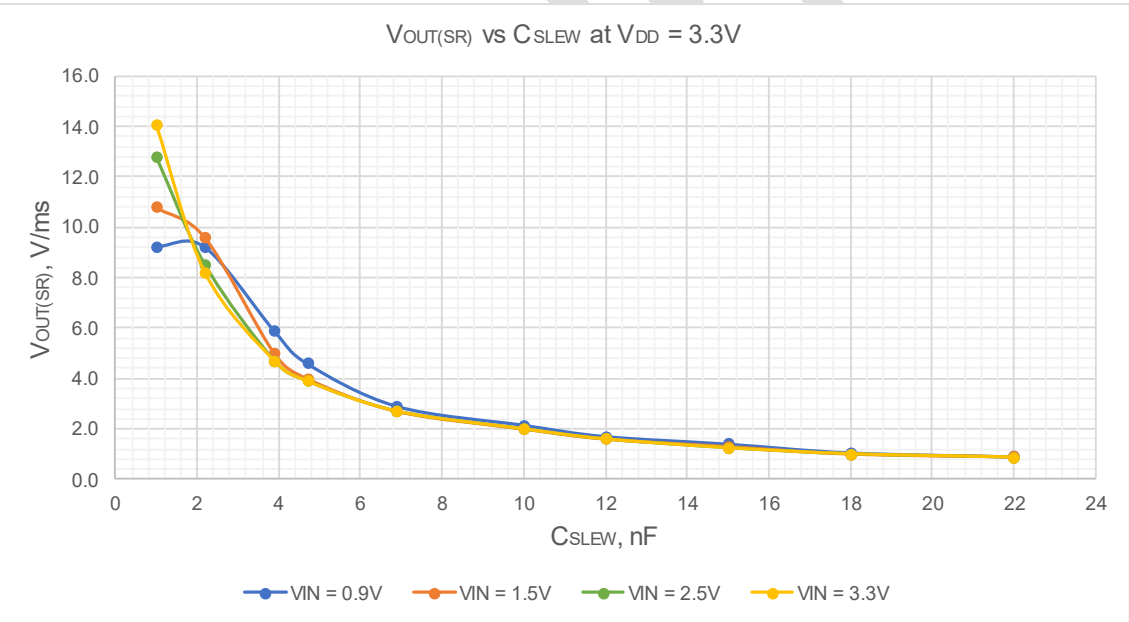


Figure 4. V_{OUT} Slew Rate vs. C_{SLEW} and V_{IN} at V_{DD} = 3.3V.

Application Information

Typical Operation

For correct operability per the AM6U1404 EC table a proper power-up sequence must be applied. Apply V_{DD} first, followed by V_{IN}, then ON signal to power-up the device. In order to control the inrush current from capacitive loads, set a desired linear output slew rate by placing a corresponding C_{SLEW} capacitor between CAP pin and GND. The greater the capacitor value at CAP pin, the slower the output ramp.

During operation, should a system fault occur, V_{IN} should be returned to Recommended Operating Conditions before the load switch is transitioned between its on and off states to reduce out-of-spec transitional stress on the device.

Some typical operation waveforms are illustrated below.

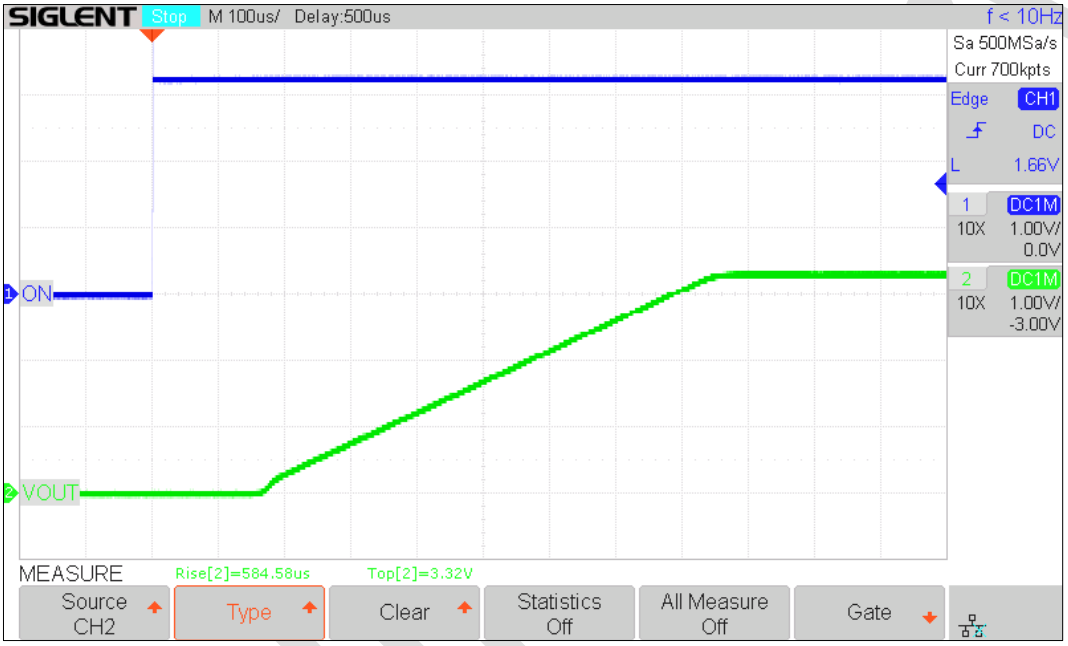


Figure 5. AM6U1404 Typical Power-Up Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, C_{OUT} = 10μF, C_{SLEW} = 3.9nF.

Figure 6. AM6U1404 Typical Power-Down Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, C_{OUT} = 10μF, C_{SLEW} = 3.9nF.

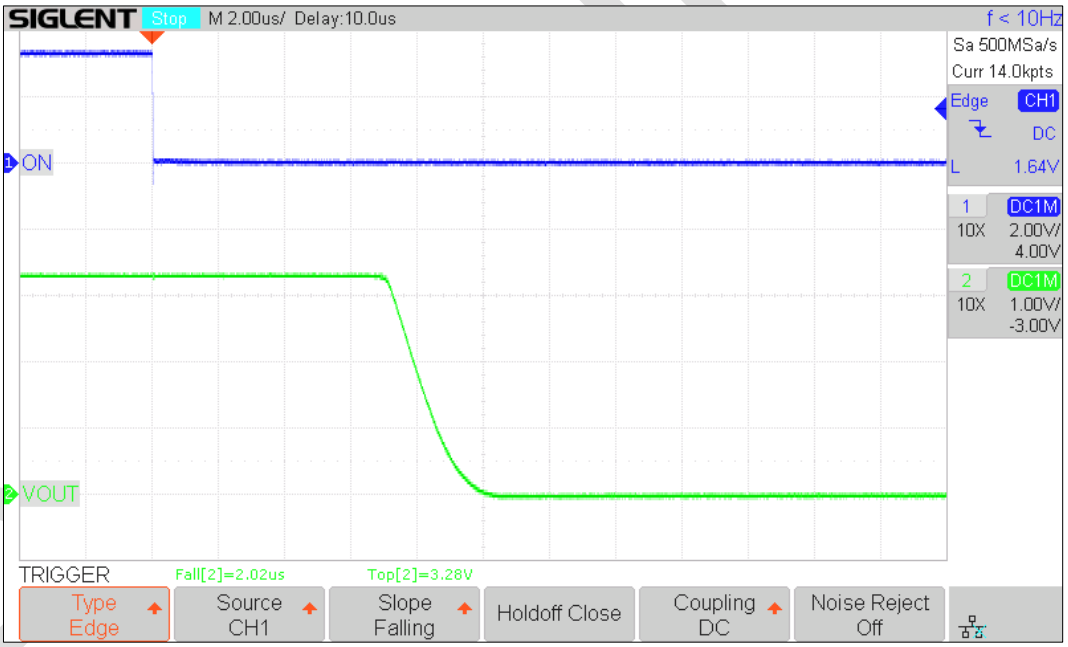


Figure 7. AM6U1404 Typical Power-Down Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, no C_{OUT}, C_{SLEW} = 3.9nF.

Overtemperature Protection

The AM6U1404 contains an overtemperature protection feature. If the internal junction temperature of the AM6U1404 reaches 125°C, such as during an overcurrent event, the FET is shut off completely so the die can cool. Once the die temperature reaches approximately 100°C Overtemperature Protection will disable and the FET will again be capable of conducting. This event will repeat for as long as the condition exists which causes the die to overheat.

Current Limiting Operation

The AM6U1404 has two types of current limiting triggered by the VOUT pin voltage.

1. Active Current Limit Mode

When voltage V_{OUT} > 300 mV the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the load switch's IACL threshold.
If a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed OTP Threshold specification, the FET is shut Off completely to allow the die to cool. When the die cools by the listed OTP Hysteresis temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

Figure 8. AM6U1404 ACL Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, C_{OUT} = 10µF, C_{SLEW} = 3.9nF. *Load Enable* signal applies an additional 0.4Ω of load.

An example of the AM6U1404 Active Current Limit is shown above. After power-up, when an overload condition occurs, the part starts to limit the current at the ACL level. Once the overload condition is removed, the part recovers to normal operation.

2. Short Circuit Current Limit Mode

The AM6U1404 also contains a short circuit limit, which will trigger in the event that V_{OUT} is externally limited to 300mV or less due to an improper solder connection or similar defect on the same node as the VOUT pin. During this event, the AM6U1404 will maintain the resistivity of the FET so as to limit the output current of the device to a typical value of 500mA.
If the Short-circuit event is resolved the AM6U1404 will continue its voltage ramp per the slew rate set by the capacitor on the CAP pin.

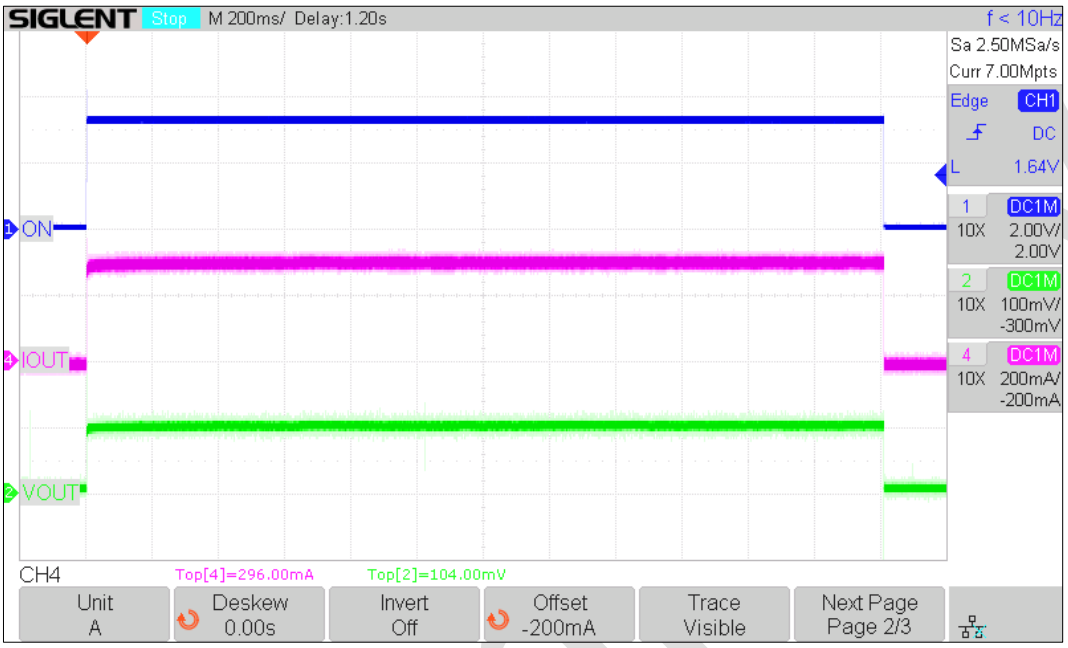
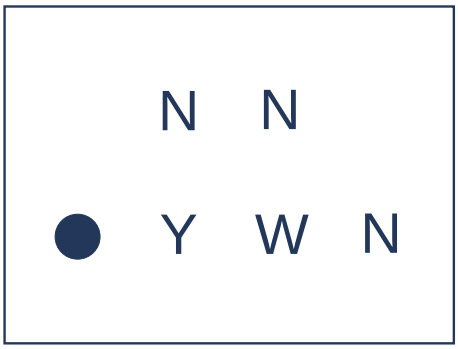


Figure 9. AM6U1404 SCL Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 0.3Ω, C_{OUT} = 10μF, C_{SLEW} = 3.9nF.

Note: Depending upon factors such as V_{IN}, the shorted value of V_{OUT}, and ambient temperature, the AM6U1404 may or may not dissipate enough power to trigger the Overtemperature Protection within the circuit. If the overtemperature protection occurs the part will shut down and retry per the Overtemperature Detection description above.

Package Top Marking



NN – Identification Code: D4
Y – Year: 0~9
W – Week: A~Z – 1~26 week
a~z – 27~52 week, z represents 52 and 53 week
N – Internal Code

Package Outline Dimensions

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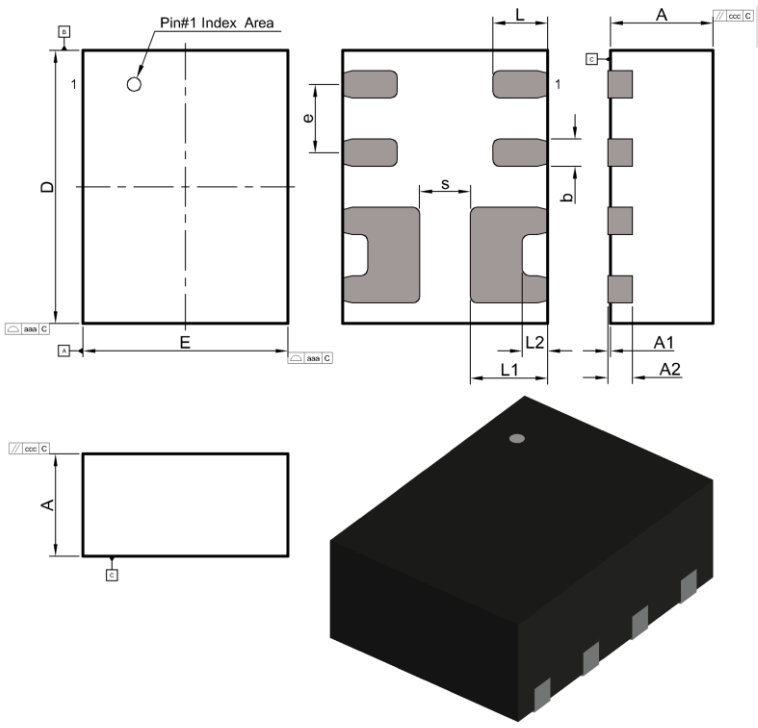

Symbol	Min.	Typ.	Max.	Symbol	Min.	Typ.	Max.
A	0.500	0.550	0.600	**L**	0.375	0.400	0.425
A1	-0.005	—	0.030	**L1**	0.515	0.565	0.615
A2	0.225	0.250	0.275	**L2**	0.135	0.185	0.235
b	0.175	0.200	0.225	**s**	—	0.370	—
D	1.950	2.000	2.050	**aaa**	—	0.050	—
E	1.450	1.500	1.550	**ccc**	—	0.050	—
e	—	0.500	—				
All Dimensions in mm							

Suggested Pad Layout

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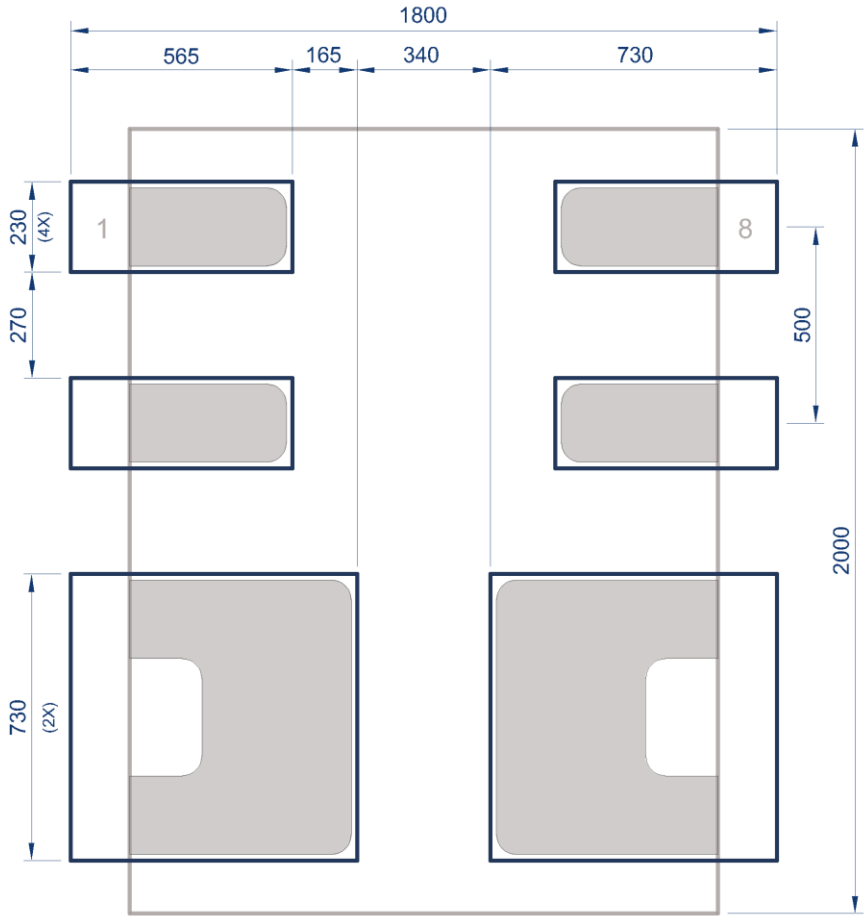
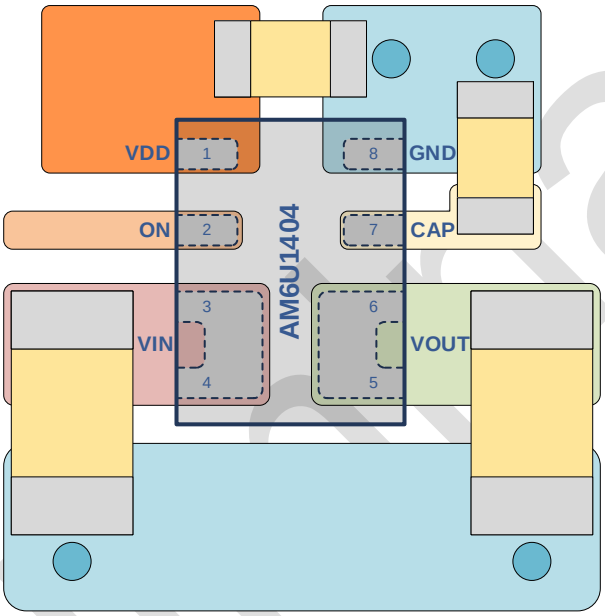


Recommended Layout

It is important to have a proper PCB layout for high-performance device operation. The list below provides some basic rules for PCB layout.

- Connect a 0.1μF capacitor from VDD pin to GND. It should be placed as close to the device as possible.
- Place high-quality low-ESR input C_{IN} (10μF min) and output C_{OUT} capacitors close to the device VIN and VOUT pins to minimize the effects of parasitic inductance.
- Make sure to have a solid Ground connection.
- All traces should be as short, wide and direct as possible.
- VIN and VOUT pins have the most heat dissipation during high-current operations. Use polygon planes and/or 2 oz. copper for VIN and VOUT connections.

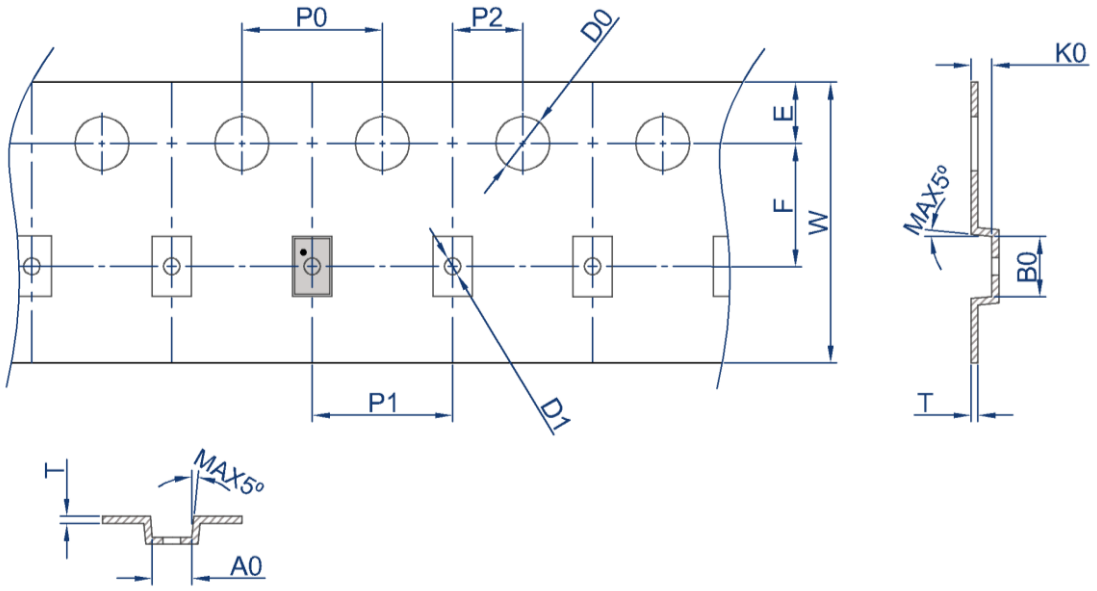
The example below illustrates described layout guidelines implementation.



Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
U-DFN2015-8	8	1.5x2.0x0.55	3,000	3,000	178/60	100	400	100	400	8	4

Package Type	A0	B0	K0	P0	P1	P2	T	D0	D1	E	F	W
U-DFN2015-8	1.68	2.18	0.7	4	4	2	0.2	1.55	0.50	1.75	3.5	8



Revision History

Date	Version	Change
November 10, 2023	Rev.001	Initial release
February 2, 2024	Rev.002	Updated EC Table, waveforms, and POD
December 18, 2024	Rev.003	Updated EC Table, waveforms, and recommended layout. Added LM information

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